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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHHAYA, SWAPNEEL	
ART UNIT	**PAPER NUMBER**
2895	

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05/13/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/541,957	FIX ET AL.	
	Examiner	Art Unit	
	SWAPNEEL CHHAYA	2895	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/11/2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-10 and 12-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-10 and 12-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/17/2007, 7/8/2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This communication is a response to the requested clarification letter dated 9/11/2008, this is a non-final rejection.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. It is unclear as to how the claimed entity of a source or drain electrode can have a width of 0 μm.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 5, 6, 9, 10, 14, 17, 3, 15, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hart (U.S. Patent 6, 362, 509).

Regarding claim 1, An organic field effect transistor (10, 20, Fig. 1) including a gate (18, 28, Fig.1) comprising:

at least

a first electrode layer forming a source or a drain electrode (14, 15, Fig. 2a, column 5 lines 15-30, 47-55) each and having multiple sides

a semiconducting layer (5, Fig. 1, column 5 lines 15-30)

an insulator layer (6, Fig. 1, column 5 lines 15-30); and

one of the source and drain electrode in the first electrode layer surrounding the respective other electrode of the first electrode layer in a two-dimensional manner with the exception of one of said sides of the other electrode (14, 15, Fig. 2a, column 5 lines 15-30, 47-55)

a second electrode layer forming a gate electrode(18, 28), the semiconductinq layer (5) exhibiting a current channel in the presence of an applied voltage and wherein the second electrode layer completely overlies the current channel and overlies a portion of the source or drain electrodes of the first electrode layer, the overlying portion with respect to the source or drain electrodes having a width solely in the range from about 0 to about 20 μm and having a length in the range of the length of the current channel to thereby minimize parasitic capacitance that otherwise might occur (Fig. 1 column 5 lines 10-40)

Hart discloses the claimed invention except for the width being “solely in the range of 0 to 20 μm”, however, as applicant has submitted in the response dated 6/16/2008, “Hart’s overlap is many orders of magnitude greater", it would have been obvious to one of ordinary skill in the art at the time the invention was made to minimize the overlap width of the electrode in order to reduce parasitic capacitance since it was known in the art that increasing the overlap region results in the disadvantage of parasitic capacitance as disclosed by Ohta et al. (U.S. Patent 7046324) in column 14 lines 10-40. The examiner would like to note that the Ohta reference is used to provide evidence that it was common knowledge in the art to minimize overlap in order to minimize parasitic capacitance. Therefore, it is still merely a result of optimization to do so.

Hart discloses the claimed invention in claims 3 and 11 except for the additionally covered part having a width in the range from 0 to 20 μm and having a length in the range of the length of the current channel. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the range from 0 to 20 μm, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

whereby a u-shaped and/or meandering current channel (Fig. 2a), which begins and ends on one of said sides of the electrode of the first electrode layer, is formed in the semiconducting layer, please note that the examiner is referring to the area between the two electrodes.

Regarding claim 2, The OFET as claimed in claim 1 wherein, in the first electrodes layer respectively bounds the other electrode layer on three of four sides (Fig.2a)

Regarding claim 5 and 14, An integrated circuit having at least two OFETs (10, 20, 30) as claimed in claim 1 wherein the at least two OFETs are arranged into a NAND (51) or NOR gate such that the one sides of the two OFETs are respectively opposite one another.(Fig. 2 column 5 lines 46-60)

Regarding claim 6, 17, the integrated circuit as claimed in claim 5; including connecting lines (39) and/or inputs (19, 29) and outputs respectively situated in a region between the one sides.(Fig. 2 column 5 lines 50-65)

Regarding claim 9, the integrated circuit as claimed in claim 5 including a through-contact (42) in said first electrode layer (Fig. 2a column 5 lines 50-60)

Regarding claim 10 The integrated circuit as claimed in claim 9, wherein the through-contact (42) extends at least to one further side of the OFET other than said one side (Fig. 2a column 5 lines 50-60)

Regarding claim 15, Hart discloses an integrated circuit having at least two OFETs (10, 20, 30) as claimed in claim 3 wherein the at least two OFETs are arranged into a NAND (51) or NOR gate such that the one sides of the two OFETs are respectively opposite one another. (Fig. 2 column 5 lines 46-60)

Regarding claim 18, the integrated circuit as claimed in claim 15; including connecting lines (39) and/or inputs 19, 29) and outputs respectively situated in a region between the one sides.(Fig. 2a column 5 lines 50-65).

3. Claims 4, 7, 8, 12, 13, 16, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hart as applied to claims 1 and 3 above in view of Ahn et Al. (U.S. Patent 6, 559, 920).

Regarding claims 4, 7, 8, 12 and 13, Hart discloses the claimed invention except for the holes and/or interruptions present in the semiconductor layer and/or between the one

sides. Ahn teaches that it is known to have holes and/or interruptions are in the semiconductor layer (202, Fig. 5B, 5D column 5 lines 9-11). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate holes and/or interruptions as taught by Ahn, since Ahn states at column 5 lines 10-11 that such a modification would decrease leakage current.

Regarding claim 16, Hart discloses an integrated circuit having at least two OFETs (10, 20, 30) as claimed in claim 4 wherein the at least two OFETs are arranged into a NAND (51) or NOR gate such that the one sides of the two OFETs are respectively opposite one another. (Fig. 2A column 5 lines 46-60)

Regarding claim 19, Hart discloses the integrated circuit as claimed in claim 5; including connecting lines (39) and/or inputs (19, 29) and outputs respectively situated in a region between the one sides. (Fig. 2a column 5 lines 50-65)

Response to Arguments

4. Applicant's arguments with respect to claims 1,2,4-10,12-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SWAPNEEL CHHAYA whose telephone number is (571)270-1434. The examiner can normally be reached on Monday- Thursday 9:30-7:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on 571-272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Fernando L. Toledo/
Primary Examiner, Art Unit 2895

SC